

**ARYA INSTITUTE OF ENGINEERING & TECHNOLOGY, JAIPUR****TIME TABLE UNIVERSITY PRACTICAL EXAMINATIONS- IV B.Tech. (VIII Semester) 2017-18**

Day/Date	Shift	ME-A	ME-B	CS-A	CS-B	CS-C
<b>Monday, 23<sup>rd</sup> April, 2018</b>	I	CAD Lab (A-1)	IE Lab (B-1)	UNPS LAB (A-1)	DIP LAB (B-1)	***
	II	CAD Lab (A-2)	IE Lab (B-2)	UNPS LAB (A-2)	DIP LAB (B-2)	***
<b>Wednesday, 25<sup>th</sup> April, 2018</b>	I	CAM Lab (A-1)	CAD Lab (B-1)	FPGA LAB (A-1)	UNPS LAB (B-1)	SEMINAR (C-1)
	II	CAM Lab (A-2)	CAD Lab (B-2)	FPGA LAB (A-2)	UNPS LAB (B-2)	SEMINAR (C-2)
<b>Saturday, 28<sup>th</sup> April, 2018</b>	I	SEMINAR (B-1)	CAM Lab (B-1)	DIP LAB (A-1)	FPGA LAB (B-1)	UNPS LAB (C-1)
	II	SEMINAR (B-2)	CAM Lab (B-2)	DIP LAB (A-2)	FPGA LAB (B-2)	UNPS LAB (C-2)
<b>Monday, 30<sup>th</sup> April, 2018</b>	I	IE Lab (A-1)	SEMINAR (B-1)	SEMINAR (A-1)	***	FPGA LAB (C-1)
	II	IE Lab (A-2)	SEMINAR (B-2)	SEMINAR (A-2)	***	FPGA LAB (C-2)
<b>Friday, 4<sup>th</sup> May, 2018</b>	I	PROJECT STAGE-II		***	SEMINAR (B-1)	DIP LAB (C-1)
	II	PROJECT STAGE-II		***	SEMINAR (B-2)	DIP LAB (C-2)
<b>Monday, 7<sup>th</sup> May, 2018</b>	I	***	***	PROJECT STAGE-II		
	II	***	***	PROJECT STAGE-II		

**Note: 1. Shift Timings for Practical Exams:- I - 9:15am - 11:45am;  
II - 12:45 pm - 3:15 pm.**

**2. Lab Batches are as per RTU Roll Nos.**

**EXAM. INCHARGE**

**DIRECTOR/PRINCIPAL**

**ARYA INSTITUTE OF ENGINEERING & TECHNOLOGY, JAIPUR****TIME TABLE UNIVERSITY PRACTICAL EXAMINATIONS- IV B.Tech. (VIII Semester) 2017-18**

Day/Date	Shift	ECE-A	ECE-B	EE-A	EE- B
<b>Monday, 23<sup>rd</sup> April, 2018</b>	<b>I</b>	RF FAB Lab (A-1)	IE & M LAB (B-1)	CBPSD Lab (A-1)	EDTC Lab (B-1)
	<b>II</b>	RF FAB Lab (A-2)	IE & M LAB (B-2)	CBPSD Lab (A-2)	EDTC Lab (B-2)
<b>Wednesday, 25<sup>th</sup> April, 2018</b>	<b>I</b>	SEMINAR (A-1)	SEMINAR (B-1)	HVE Lab (A-1)	CBPSD Lab (B-1)
	<b>II</b>	SEMINAR (A-2)	SEMINAR (B-2)	HVE Lab (A-2)	CBPSD Lab (B-2)
<b>Saturday, 28<sup>th</sup> April, 2018</b>	<b>I</b>	VLSI LAB (A-1)	RF FAB Lab (B-1)	SEMINAR (A-1)	HVE Lab (B-1)
	<b>II</b>	VLSI LAB (A-2)	RF FAB Lab (B-2)	SEMINAR (A-2)	HVE Lab (B-2)
<b>Monday, 30<sup>th</sup> April, 2018</b>	<b>I</b>	IE & M LAB (A-1)	VLSI LAB (B-1)	EDTC Lab (A-1)	SEMINAR (B-1)
	<b>II</b>	IE & M LAB (A-2)	VLSI LAB (B-2)	EDTC Lab (A-2)	SEMINAR (B-2)
<b>Friday, 4<sup>th</sup> May, 2018</b>	<b>I</b>	PROJECT STAGE -II		***	
	<b>II</b>	PROJECT STAGE -II		***	
<b>Monday, 7<sup>th</sup> May, 2018</b>	<b>I</b>	***		PROJECT STAGE -II	
	<b>II</b>	***		PROJECT STAGE -II	

**Note: 1. Shift Timings for Practical Exams:- I - 9:15am - 11:45am; II - 12:45 pm - 3:15 pm.**

**2. Lab Batches are as per RTU Roll Nos.**

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